Claims:

1. A method for manufacturing a printed circuit board element, wherein starting from a printed circuit board substrate (12) with at least one conductor layer (13), this conductor layer is structured and noble metal (16) is applied thereon, characterised in that the conductor layer (13) is roughened in the surface area, and noble metal (16) is applied as a layer on essentially the whole structured, roughened conductor layer (13), wherein the surface of the noble metal layer is provided with a corresponding roughness (8').

2. A method according to claim 1, characterised in that the surface of the conductor layer (13) is roughened with a roughness (8) in the range of between 0.05 µm and 5 µm, e.g. 0.3 µm and 3 µm, preferably 0.5 µm and 1 µm.

3. A method according to claim 1 or 2, characterised in that the surface of the conductor layer (13) is roughened by chemical etching.

4. A method according to claim 1 or 2, characterised in that the surface of the conductor layer (13) is roughened by ionic etching.

5. A method according to claim 1 or 2, characterised in that the surface of the conductor layer (13) is roughened by mechanical processing.

6. A method according to claim 1 or 2, characterised in that the surface of the conductor layer (13) is roughened by electroplating.

7. A method according to any one of claims 1 to 6, characterised in that the noble metal layer (16) is applied on the conductor layer (13) with a thickness of between 0.02 µm and 1 µm, preferably 0.02 µm and 0.5 µm.

8. A method according to any one of claims 1 to 7, characterised in that the noble metal layer (16) is applied on the conductor layer (13) in chemical-currentless manner.

9. A method according to any one claims 1 to 7, characterised in that the noble metal layer (16) is applied on the conductor layer (13) by electroplating.

10. A method according to any one of claims 1 to 7, characterised in that the noble metall layer (16) is applied on the conductor layer (13) by cathodic evaporation.

11. A method according to any one of claims 1 to 7, characterised in that the noble metall layer (16) is applied on the conductor layer (13) by sputtering.

12. A method according to any one of claims 1 to 11, characterised in that a layer made of at least one metal from the group comprising silver, gold, palladium, platinum and nickel, is used as the noble metal layer (16).

13. A method according to any one of claims 1 to 12, characterised in that after having applied the noble metal layer (16) on the roughened conductor layer (13) at least one electric component (4) is mounted in the areas of the surface-roughened noble metal layer (16).

14. A method according to claim 13, characterised in that the electric component (4) is a resistor, e.g. a PTF resistor.

15. A method according to any one of claims 1 to 14, characterised in that after having applied the noble metal layer (16) on the roughened conductor layer (13) as well as, optionally, after having mounted the electric component (4) on the upper side of the printed circuit board substrate (12), a further printed circuit board structure (1') is applied together with the surface-roughened noble metal layer

(16) and thus a pressing to a multilayer is yielded.

16. A method acccording to any one of claims 1 to 14, characterised in that after having applied the noble metal layer (16) on the roughened conductor layer (13) as well as, optionally, after having mounted the electric component (4) on the upper side of the printed circiut board substrate (12), a solder stop mask is mounted together with the surface-roughened noble metal layer (16).

17. A method according to any one of claims 1 to 16, characterised in that a printed circuit board substrate (12) with two conductor layers (13; 13') is used, wherein at least one conductor layer is structured and roughened.

18. A method according to any one of claims 1 to 17, characterised in that, after having been structured, the conductor layer is roughened in the surface area.

19. A printed circuit board element with at least one structured conductor layer (13) on a substrate (12), and with noble metal (16) on the conductor layer (13), characterised in that the conductor layer (13) has a roughened surface (8) and that said layer has a surface-rough noble metal layer (16) serving as contact promoting and stabilizing layer, on the one hand, and as adherence promoting layer, on the other hand.

20. A printed circuit board element according to claim 19, characterised in that a further printed circuit board structure (1') is provided on the surface-rough noble layer (16), forming a multilayer configuration.

21. A printed circuit board element according to claim 19, characterised in that a solder stop mask is mounted on to the surface-rough noble metal layer (16).

22. A printed circuit board element according to any

one of claims 19 to 21, characterised in that at least one electric component (4) is mounted on the surface-rough noble metal layer (16).

23. A printed circuit board element according to claim 22, characterised in that the electric component (4) is a resistor, e.g. a PTF resistor.

24. A printed circuit board element according to any one of claims 19 to 23, characterised in that the conductor layer (13) and the noble metal layer (16), respectively, has a surface roughness (8; 8') of between 0.05 µm and 5 µm, e.g. 0.3 µm and 3 µm, preferably 0.5 µm and 1 µm.

25. A printed circuit board element according to any one of claims 19 to 24, characterised in that the noble metal layer (16) has a thickness of between 0.02 µm and 1 µm, preferably 0.02 µm and 0.5 µm.

26. A printed circuit board element according to any one claims 19 to 25, characterised in that the noble metal layer (16) has at least one metal selected from the group consisting of silver, gold, palladium, platinum and nickel.

27. A printed circuit board element acccording to any one of claims 19 to 26, characterised in that the substrate (12) has two structured conductor layers (13, 13'), wherein on at least one noble metal layer (16) is applied.